

REMARKS

Claims 1-8 and 14-61 are canceled. Claims 9-13 and 62-65 are pending in the present application.

Claim 9 recites a memory device comprising "a gate stack pair with a space between them defining a contact opening" and "a vertical oxide spacer adjacent to each gate stack of said gate stack pair" wherein the "*vertical oxide spacer is recessed from a top surface of each gate stack.*" Emphasis added. The Advisory Action mailed on November 28, 2006 argues that the "sidewalls are recessed in Fig. 3" and that, therefore, Fig. 3 is prior art over the claimed invention. Figure 3 "illustrates a problem that occurs when the self-align contact etch 17 is misaligned so as to hit a gate stack" (Specification at para. [0008]) but does not show that the spacer is "recessed from a top surface of the gate stack," as recited in claim 9. In fact, the spacer 11 shown in Figure 3 still runs the entire length of the gate stack, and only the *nitride spacer 14* is etched to a level that is recessed from the top surface of the gate stack. Thus, Figure 3 is not prior art over the claimed invention.

In view of the above remarks, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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